Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1. (Currently amended) An image processing system comprising:

a first processing layer operative to perform object-independent processing in a real time physical environment, wherein said object-independent processing is further operative to include a plurality of processors corresponding to the first processing layer, and wherein each of the plurality of the processors is associated with a different one of pixels of an image frame in order to perform per-pixel processing in order to enhance object distinguishing in a higher processing layer, said first processing layer being instantiated as a real-time-capable MPP SIMD;

a second processing layer on top of said first processing layer and operative to perform object-dependent and pixel-independent processing in said real-time physical environment to obtain a dynamic feature set for use in object recognition, said dynamic feature set comprising object perimeters and static and dynamic object features, including linear and non-linear motion parameters, said second processing layer being instantiated as a real-time-capable SMP matrix multiplication processor combined with an SMP-type Fast Fourier Transform processor; and

a third processing layer on top of said second processing layer and operative in real time to perform object recognition and association by employing said dynamic feature set against an object to be recognized.

2-5. Canceled.

6. (Original) The image processing system of claim 1 wherein each of the plurality of the processors operative to perform object independent processing is enabled to perform a unified and symmetric processing of N dimensions in space and one dimension in time.

7. (Currently amended) The image processing system of claim ~~1~~ 6 further comprising:

an image capturing block.

8. (Original) The image processing system of claim 7 wherein the plurality of processors are formed on a first semiconductor substrate different from a second semiconductor substrate on which the image capturing block is formed.

9. (Previously presented) The image processing system of claim 8 further comprising:

a realignment buffer operative to realign the data received from first and second analog-to-digital converters disposed in the image capturing block.

10. (Currently amended) A method for processing images comprising:

performing object-independent processing in a first processing layer in a real time physical environment by means of a plurality of real-time-capable processors, each processor associated with a different one of pixels of an image frame being processed, in order to enhance object distinguishing in a higher second processing layer;

performing object-dependent and pixel-independent processing in a second processing layer on top of said first processing layer in said real-time physical environment in order to guarantee to obtain a dynamic feature set in real time for use in object recognition, said dynamic feature set comprising object perimeters and static and dynamic object features, including linear and non-linear motion parameters; and

performing in real time object recognition and association in a third processing layer on top of said second processing layer by employing said dynamic feature set against an object to be recognized.

11. Canceled.

12. (Previously presented) The method of claim 10 further comprising:

performing object-dependent processing by a symmetric multi-processor.

13. (Previously presented) The method of claim 12 further comprising:

performing object independent processing by a plurality of processors that form a massively parallel processing system.

14. (Original) The method of claim 13 wherein the massively parallel processing system is a systolic array type massively parallel processing system.

15. (Original) The method of claim 14 further comprising:

configuring the systolic array massively parallel processing system as a single-instruction multiple-data system.

16. (Currently amended) The method of claim ~~11~~ 15 wherein each of the plurality of the processors is enabled to perform a unified and symmetric processing of N dimensions in space and one dimension in time.

17. (Currently amended) The method of claim ~~11~~ 16 further comprising:

capturing the image frame on a first semiconductor substrate that is different from a second semiconductor substrate on which the plurality of processors are formed.

18. (Currently amended) The method of claim 17 further comprising:

converting analog data corresponding to the image frame to digital data; and

realigning the converted digital data.